12-27-99

A

Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

JC544 U.S. PTO 12/23/99

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P7604 Total Pages 2

First Named Inventor or Application Identifier Lloyd L. Pollard II

Express Mail Label No. EL034433500US

JC564 U.S. PTO 09/471220 12/23/99

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 23)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 3)

4. X Oath or Declaration (Total Pages 4 (unsigned))
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. __ Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __ Other: _____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _____

18. **Correspondence Address**
_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)
or
__X__ Correspondence Address Below

NAME Aloysius T.C. AuYeung
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
ADDRESS 12400 Wilshire Boulevard
Seventh Floor
CITY Los Angeles STATE California ZIP CODE 90025-1026
Country U.S.A. TELEPHONE (503) 684-6200 FAX (503) 684-3245

UNITED STATES PATENT APPLICATION

for

DYNAMICALLY CONFIGURABLE THERMAL MANAGEMENT

Inventors:

Lloyd L. Pollard II
Nitin B. Gupte

prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026
(503) 684-6200

File No.: 42390.P7604

Express Mail Label No.: EL034433500US

DYNAMIC THERMAL MANAGEMENT FOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to thermal management. More specifically, the present invention relates to dynamic thermal management of integrated circuits within a computer system.

2. BACKGROUND INFORMATION

The continued trend in integrated circuit (IC) technology is to increase operating frequencies, data transfer rates, and the average number of transistors per IC, while decreasing IC package sizes. Unfortunately, as IC performance levels increase and package sizes decrease, the power density of the ICs increase resulting in higher operating temperatures within each IC. If such operating temperatures are not controlled or managed, the ICs may reach or exceed critical temperature thresholds causing damage and even operational failure to the ICs.

Since system integrators may utilize a variety of ICs within a variety of chassis environments, the resulting thermal characteristics and associated cooling requirements for each system may vary greatly from one assembled system to another. Conventionally, the cooling requirements and associated performance limitations for each system were not determined independently given the specific thermal characteristics of the system. Rather, the cooling requirements and associated

performance limitations were determined based upon a least optimal thermal environment (or "lowest common denominator" system). Accordingly, ICs located within thermally efficient environments that were capable of operating at higher frequencies without overheating, were penalized by having performance limits set artificially low based upon less thermally efficient system environments. By artificially setting performance limits low, valuable bandwidth and/or processing power is wasted.

SUMMARY OF THE INVENTION

A thermal management method is disclosed. The method includes determining a maximum sustainable power level for an integrated circuit based upon characteristic data, translating the maximum sustainable power level into a maximum performance characteristic, and adjusting operation of the integrated circuit such that the maximum performance characteristic is not exceeded.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more fully understood from the detailed description given below and from the accompanying drawings of various embodiments of the invention, which, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

Figure 1 is a block diagram illustrating one embodiment of an arrangement for providing dynamic thermal management of an IC.

Figure 2 is a flow diagram illustrating the operation of a Basic Input/Output System as it relates to one embodiment of the present invention.

Figure 3 is a graph illustrating the relationship between a given power input and a corresponding temperature output of an IC.

DETAILED DESCRIPTION

The present invention provides for dynamic thermal management of integrated circuits, including memory modules, within a computer system. The thermal management methodology described herein closely couples software operation to hardware operation of the computer system, and allows each system to run at near optimum performance levels without exceeding specified temperature thresholds. In order to achieve such results, the present invention relates physical characteristics of the integrated circuit with physical characteristics of the internal chassis environment, and translates this relationship into a maximum software performance setting. The system is then able to monitor and adjust software performance such that the determined maximum performance setting is not exceeded.

In the following description, various aspects of the present invention will be described, and various details will be set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some or all aspects of the present invention, and the present invention may be practiced without the specific details. In other instances, well known features are omitted or simplified in order not to obscure the present invention.

Parts of the description will be presented using terminology commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. Additionally, parts of the description will also be presented in terms of operations

performed through the execution of programming instructions, using terms such as determining, selecting, processing and so on. As well understood by those skilled in the art, these operations are often accomplished through storing, transferring, combining, or otherwise manipulating electrical, magnetic, and/or optical signals.

Various operations will be described as multiple discrete steps performed in turn in a manner that is most helpful in understanding the present invention. However, the order of description should not be construed as to imply that these operations are necessarily performed in the order they are presented, or even order dependent. Lastly, repeated usage of the phrase "in one embodiment" does not necessarily refer to the same embodiment, although it may.

Figure 1 is a block diagram illustrating one embodiment of an arrangement for providing dynamic thermal management of an IC. System 100 is shown including BIOS 110, central processing unit (CPU) 130, and memory module 140, all of which are coupled together via chipset 120. Although in one embodiment, system 100 represents a general purpose computer system, the invention described herein should not be read as being limited for use solely within a general purpose computer system.

Chipset 120 represents one or more general and/or special purpose data control devices known in the art to route data and optimize performance between various functional components of system 100.

CPU 130 represents a general purpose microprocessor known in the art to process data. In one embodiment, CPU 130 is a processor from the PENTIUM® (e.g., PENTIUM®, PENTIUM® II, PENTIUM® III) family of processors available from Intel Corporation of Santa Clara, California. It will be apparent to one skilled in the art, however, that a variety of other general and/or special purpose processors could also be used.

BIOS 110 represents a nonvolatile memory device, such as for example, an electrically erasable programmable read only memory (EEPROM) or a flash memory, having a basic input/output system stored therein. In one embodiment, BIOS 110 includes a variety of system environment characteristics, including for example, thermal characteristics. In one embodiment, the thermal characteristics are set in BIOS 110 by a system integrator for example, to reflect the specific thermal environment of a given system as determined, at least in part, by the configuration of the system. Such thermal characteristics can include, but are not limited to the local airspeed within a system chassis, the ambient air temperature within the chassis, the spacing of integrated circuits such as memory modules and processors within the chassis, and so forth. Although such environmental characteristics may be manually set within BIOS 110, various automated mechanisms including airspeed sensors and temperature sensors may instead be used to automatically provide at least a portion of such environmental characteristic data to BIOS 110.

Memory module 140 represents any of variety of volatile data storage devices known in the art to temporarily store data. Such data storage devices can include random access memory (RAM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and the like. In one embodiment, memory module 140 is an RDRAM® memory module available from Rambus Inc., of Mountain View, California. In one embodiment, memory module 140 further includes ROM 145 which represents a nonvolatile data storage device, such as an EEPROM or flash memory, to store module design characteristic data specific to memory module 140. Such module design characteristic data can indicate the associated memory module type, module organization, module timing parameters, and the like. In one embodiment of the present invention, ROM 145 is a serial presence detect (SPD) device that stores memory module design characteristics including the number of devices on the module, active, idle, and standby power consumption levels of each device on the module, substrate height, heat spreader design data, a maximum allowable junction temperature, and so forth.

BIOS 110 utilizes a combination of thermal environment characteristics and memory module design characteristics to determine a maximum sustainable power level for an integrated circuit, such as memory module 140. For the purposes of this disclosure, "maximum sustainable power level" is defined as an amount of operational power that an integrated circuit can dissipate given a particular thermal environment so as to not exceed specified minimum and/or maximum temperature thresholds. In embodiments where the integrated circuit is an RDRAM® memory module, a maximum

sustainable power level for the module may be determined according to the following equation 1:

$$Px = \frac{[(Tj - Ta) - (B \times Pact\_i + C \times Pstdby + D \times Pnap)]}{A} \quad \textbf{(EQ. 1)}$$

Unlike most other memory modules, RDRAM® memory modules comprise multiple discrete memory devices that are individually addressable by a host system. Due to this distinction, only a select one of the various memory devices will be active at any given time. The remainder of the memory devices that are not in an active state assume a variety of power management modes, including a standby mode and a nap mode, as determined by a given power distribution model for the module ("pooling policy"). In one embodiment, the pooling policy is fixed, whereas in other embodiments, the pooling policy can be dynamically determined by BIOS 110 (using equation 1 for example) so as to maximize bandwidth given a maximum sustainable active device power.

Referring to Equation 1, (Px) represents the maximum sustainable power level which is to be determined for the given integrated circuit (e.g. memory module 140), Tj represents the junction temperature of the specific memory module, Ta represents the ambient temperature within a system (e.g. system 100) chassis, Pact_i represents the power level for the active idle device, P$stdby$ represents the power level(s) for one or

more devices in standby mode, and P*nap* represents the power level(s) for one or more devices in nap mode.

Multipliers A, B, C and D represent influence coefficients specific to the given system being analyzed. The influence coefficients may be determined using principles known in the art based upon various environmental characteristics of the system including airflow rates, specific module layout, and integrated circuit packaging, as well as chassis layout, and motherboard layout. In one embodiment, the influence coefficients are stored in BIOS 110 and are referenced by the BIOS for use in determining the sustainable power level for an associated integrated circuit. In one embodiment, BIOS 110 includes influence coefficients for a variety of possible system platform in addition to the system platform within which BIOS 110 is located. In such an embodiment, BIOS 110 can, for example, access the proper influence coefficients through the use of a lookup table.

Once BIOS 110 determines the maximum sustainable power level for the integrated circuit, it translates this power level into a maximum performance characteristic. In one embodiment, the maximum performance characteristic represents an average allowable sustained data transfer rate or "bandwidth" such that during normal operation, the integrated circuit (or memory module) does not exceed specified temperature thresholds. Given the maximum sustainable power level (Px), the average allowable bandwidth (BW) may be calculated based upon the following equation 2:

$$BW = \frac{[Px \times Peak\_bandwidth]}{Max\_Device\_power} \qquad \textbf{(EQ. 2)}$$

Referring to equation 2, *Peak_bandwidth* represents a fixed value that refers to the maximum threshold bandwidth that the specific integrated circuit technology is capable of handling. Such information is readily available and can be programmed within a ROM for automatic retrieval by BIOS 110. For example, an RDRAM® memory module and/or memory subsystem has a known maximum bandwidth of 1.6 Gigabytes per second (Gb/s) which can be utilized by BIOS 110 to determine *BW* for a given RDRAM® module. The *Max_Device_power* is a value, provided by the manufacturer of the integrated circuit, that specifies the maximum amount of power a given active device can dissipate. In an embodiment where the integrated circuit is an RDRAM® memory module, *Max_Device_power* refers to the maximum power the single active device can dissipate at peak bandwidth without being damaged. In one embodiment, the values representing both *Peak_bandwidth* and *Max_Device_power* are stored in a ROM that is accessible to BIOS 110. In an embodiment where the integrated circuit is a memory module, the *Peak_bandwidth* and *Max_Device_power* are stored in a ROM, such as ROM 145, located on the memory module.

Once the maximum performance characteristic (e.g. bandwidth) of the integrated circuit is determined, the system adjusts operation of the integrated circuit so as to keep operating temperatures within a specified range. In one embodiment, BIOS 110 adjusts operation of memory module 140 to maintain operating temperatures within a specified range, whereas in an alternative embodiment, chipset 120 may adjust the operation of

memory module 140 to maintain such a temperature range. In an embodiment where the maximum performance characteristic represents the allowable sustained data transfer rate through memory module 140, BIOS 110 monitors the total number of reads and writes experienced by memory module 140. As long as the total number of memory reads/writes does not exceed a threshold amount within a specified time frame, operation of memory module 140 is not affected. If, however, the total number of memory reads/writes does exceed a threshold amount within a specified time frame, then BIOS 110 attempts to decrease performance of memory module 140. In one embodiment, BIOS 110 decreases performance of memory module 140 by suspending further reads/writes from/to memory module 140 for a period of time. It will be apparent to one skilled in the art, however, that other such methods may be implemented to decrease performance.

Figure 2 is a flow diagram illustrating one embodiment of the operation of a dynamic thermal management system. In accordance with one embodiment of the present invention, BIOS 110 accesses characteristic data representing the specific thermal environment of the computer system within which BIOS 110 is located (202). In one embodiment, the characteristic data is stored within BIOS 110, whereas in other embodiments, the characteristic data may be stored within a memory device other than BIOS 110. BIOS 110 additionally accesses module design characteristics indicating the specific design implementation of memory module 140 (204). In one embodiment, the module design characteristics are stored within ROM 145 of memory module 140.

Given specific thermal system environment characteristics (including airspeed and air temperature), module design characteristics (including the number of devices on the memory module), and a usage model (including the number of active devices, active idle devices, and standby devices on the memory module, as well as the power dissipated by each device), BIOS 110 determines the maximum sustainable power that the single active device can dissipate without exceeding a specified temperature range (206).

Once BIOS 110 determines the maximum sustainable active device power, it translates this value into a maximum performance characteristic (208). In one embodiment, the maximum performance characteristic represents a maximum allowable sustained data transfer rate for memory module 140. Once the maximum performance characteristic is determined, BIOS 110 adjusts operation of the memory module accordingly such that the determined maximum performance characteristic is not exceeded (210).

In the above description, the maximum performance characteristic of an active device was described in terms of the average allowable bandwidth (BW) and the maximum sustainable power level (Px) for the device. The length of time for which the device may transfer data at a predetermined maximum rate ("burst rate", wherein burst rate = peak bandwidth) may also be obtained given the maximum sustainable power level (Px) for the device.

Typically, a change in power input into an IC results in a corresponding change in temperature of the IC. Thus, if power input into an integrated circuit is controlled, the temperature of the IC may be estimated based on the known response characteristics. In an IC, temperature changes in response to corresponding input power changes are driven by the thermal time constant of each integrated circuit package. Such thermal time constants may readily be ascertained according to methods known in the art. Given the specific thermal time constant of an IC, the initial power state of the IC, the maximum sustainable power level (Px) for the IC, and an initial ambient temperature, the length of time for which the integrated circuit can operate at its burst rate/peak bandwidth may be determined such that the IC temperature is maintained within some threshold range.

Figure 3 is a graph illustrating the relationship between a given power input and a corresponding temperature output of an IC. At time t1, the IC exists in an initial power state (level 2). As long as this initial power state is maintained, the corresponding temperature of the IC remains unchanged. When the power input of the IC is increased at time t2 (from level 2 to level 4 for example), the temperature of the IC asymptotically increases towards a temperature indicated by level D. At time t3, the power input is decreased to yet another level (level 3). As the power input is decreased at t3, the IC temperature asymptotically decreases to a corresponding temperature level C. At time t5, the power input is decreased to a power level (level 1) that is less than the initial power level of the IC. In such a case, the temperature also decreases (asymptotically) to a level (level A) that is less than the initial temperature.

Although in the above description, operation of the present invention has primarily been described with respect to memory modules, the present invention is equally applicable to a variety of integrated circuits including for example, CPU 130. Rather than utilizing memory module design characteristics, BIOS 110 may equivalently utilize processor design characteristics stored within CPU 130 or some identified data storage device.

Thus, a system for dynamic thermal management of integrated circuits has been described. In the above description, a value representing the maximum sustainable power level for an active device within a system was determined. That power level value was then utilized to determine a maximum operational bandwidth for the device such that under normal conditions, the device would not exceed established operational temperature thresholds. Additionally, the maximum sustainable power level for a device was utilized to determine a length of time for which the device can operate at a maximum transfer rate ("burst rate") such that the device would not exceed established operational temperature thresholds.

Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the

claims which in themselves recite only those features regarded as essential to the invention.

CLAIMS

What is claimed is:

1. A method comprising:

determining a maximum sustainable power level for an integrated circuit based upon characteristic data;

translating the maximum sustainable power level into a maximum performance characteristic; and

adjusting operation of the integrated circuit such that the maximum performance characteristic is not exceeded.

2. The method of claim 1, wherein determining a maximum sustainable power level for the integrated circuit based upon environmental characteristics further comprises determining a maximum sustainable power level for the integrated circuit based upon thermal environment characteristics of a system containing the integrated circuit.

3. The method of claim 2, wherein the thermal characteristics are stored within a BIOS.

4. The method of claim 1, wherein determining a maximum sustainable power level for the integrated circuit based upon environmental characteristics further comprises determining a maximum sustainable power level for the integrated circuit based upon design characteristics of the integrated circuit.

5. The method of claim 4, wherein the design characteristics are stored within the integrated circuit.

6. The method of claim 1, wherein the integrated circuit comprises a memory module.

7. The method of claim 6, wherein the memory module comprises a RDRAM memory module.

8. The method of claim 1, wherein the maximum performance characteristic comprises a maximum allowable data transfer rate.

9. The method of claim 8, wherein adjusting operation of the integrated circuit further comprises:

monitoring an amount of data transferred to and/or from the integrated circuit; and

reducing the amount of data transferred if the amount of data transferred results in a data transfer rate that exceeds the maximum allowable data transfer rate.

10. The method of claim 8, wherein adjusting operation of the integrated circuit further comprises determining an amount of time for which the maximum allowable data transfer rate may be sustained.

11. A apparatus comprising:

first circuitry to:

determine a maximum sustainable power level for an integrated circuit based upon environmental characteristics;

translate the maximum sustainable power level into a maximum performance characteristic; and

adjust operation of the integrated circuit such that the maximum performance characteristic is not exceeded.

12. The apparatus of claim 11, wherein the environmental characteristics include integrated circuit design characteristics stored within the integrated circuit.

13. The apparatus of claim 11, wherein the environmental characteristics include thermal characteristics stored within the apparatus.

14. The apparatus of claim 11, wherein the integrated circuit comprises a memory module.

15. A system comprising:

an integrated circuit; and

a BIOS coupled to the integrated circuit to:

determine a maximum sustainable power level for the integrated circuit based upon environmental characteristics,

translate the maximum sustainable power level into a maximum performance characteristic, and

adjust operation of the integrated circuit such that the maximum performance characteristic is not exceeded.

16. The system of claim 15, wherein the integrated circuit comprises a memory module having at least a portion of the environmental characteristics stored thereon.

17. The system of claim 15, wherein the environmental characteristics include thermal characteristics of the system.

18. The system of claim 15, wherein the maximum performance characteristic comprises a maximum allowable data transfer rate.

19. An article of manufacture comprising a machine readable medium having a plurality of machine readable instructions stored thereon, wherein the instructions, when executed by a processor, cause the processor to:

determine a maximum sustainable power level for an integrated circuit based upon environmental characteristics;

translate the maximum sustainable power level into a maximum allowable data transfer rate;

adjust operation of the integrated circuit such that the maximum allowable data transfer rate is not exceeded.

20. The article of manufacture of claim 19, further comprising instructions that, when executed by a processor, cause the processor to adjust operation of the integrated circuit by determining an amount of time for which the maximum allowable data transfer rate may be sustained.

ABSTRACT

The present invention provides for dynamic thermal management of integrated circuits, including memory modules, within a computer system. The thermal management methodology described herein closely couples software operation to hardware operation of the computer system, and allows each system to run at near optimum performance levels without exceeding specified maximum temperature thresholds. In order to achieve such results, the present invention relates physical characteristics of the integrated circuit with physical characteristics of the internal chassis environment, and translates this relationship into a maximum software performance setting. The system monitors and adjusts software performance such that the maximum performance setting is not exceeded.

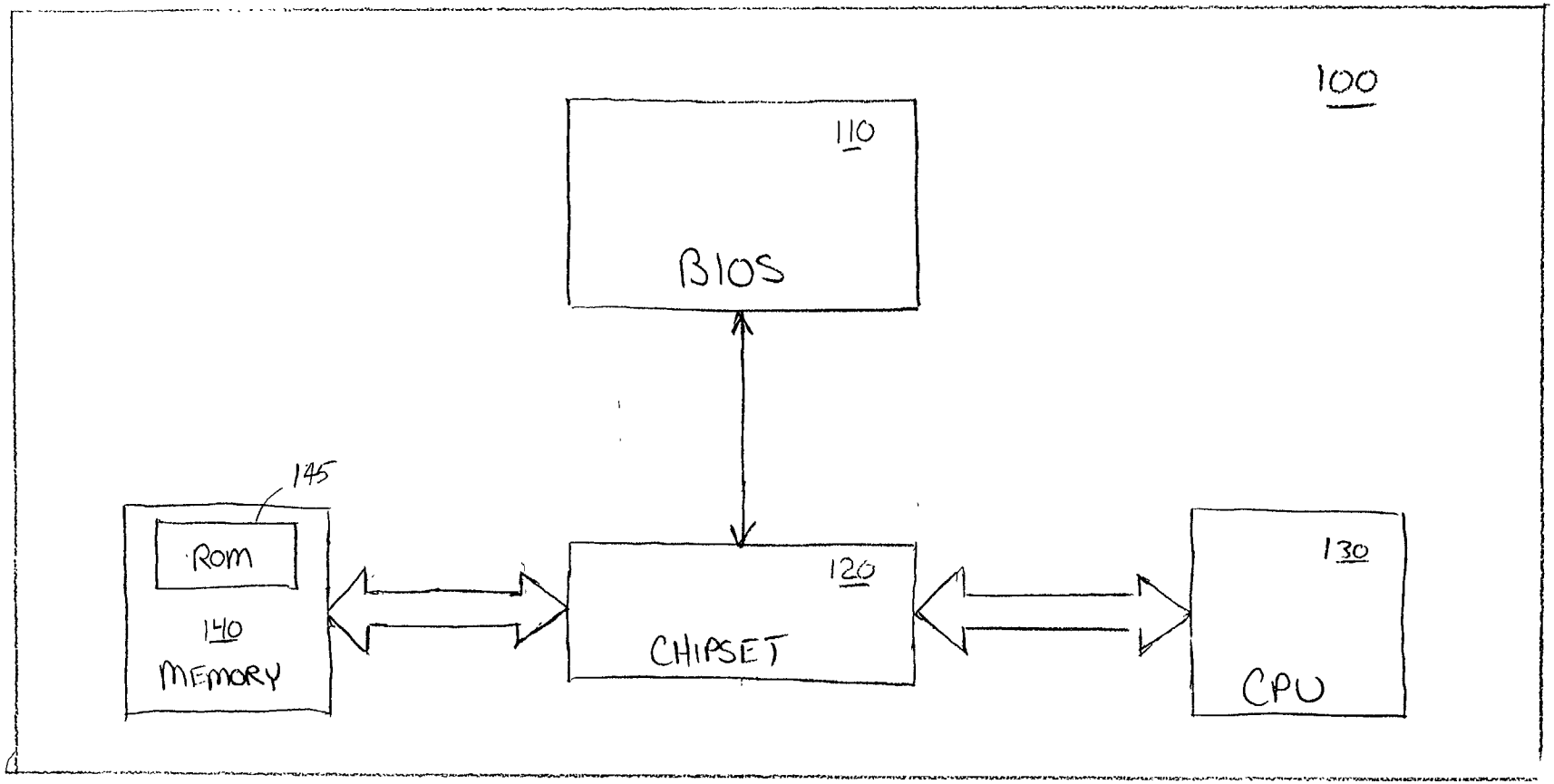


FIG 1

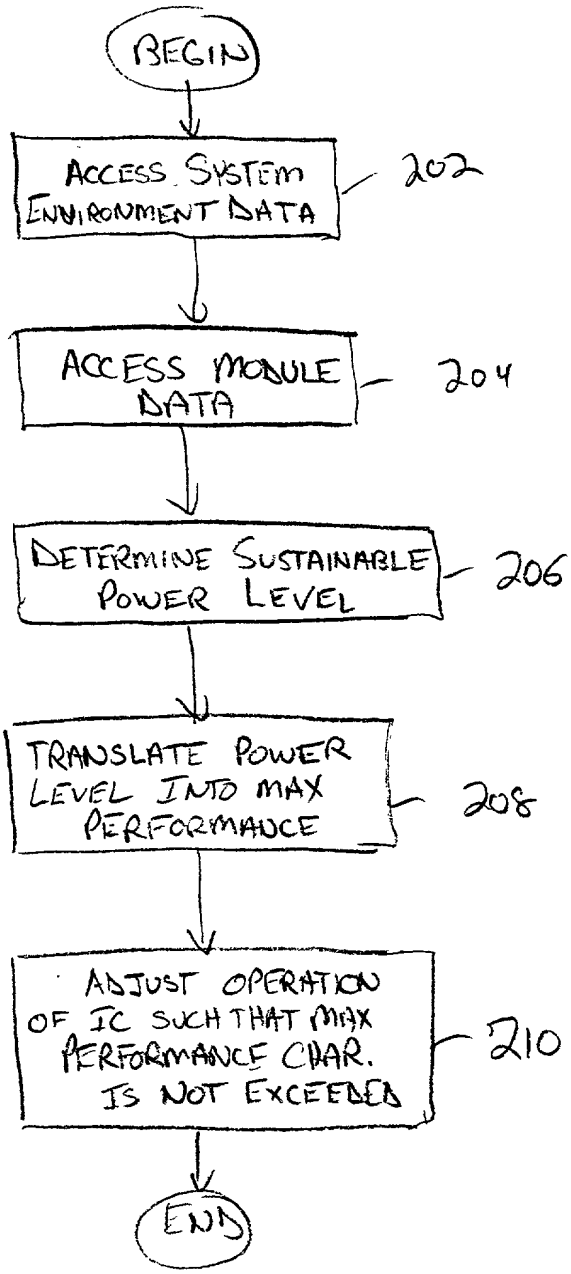
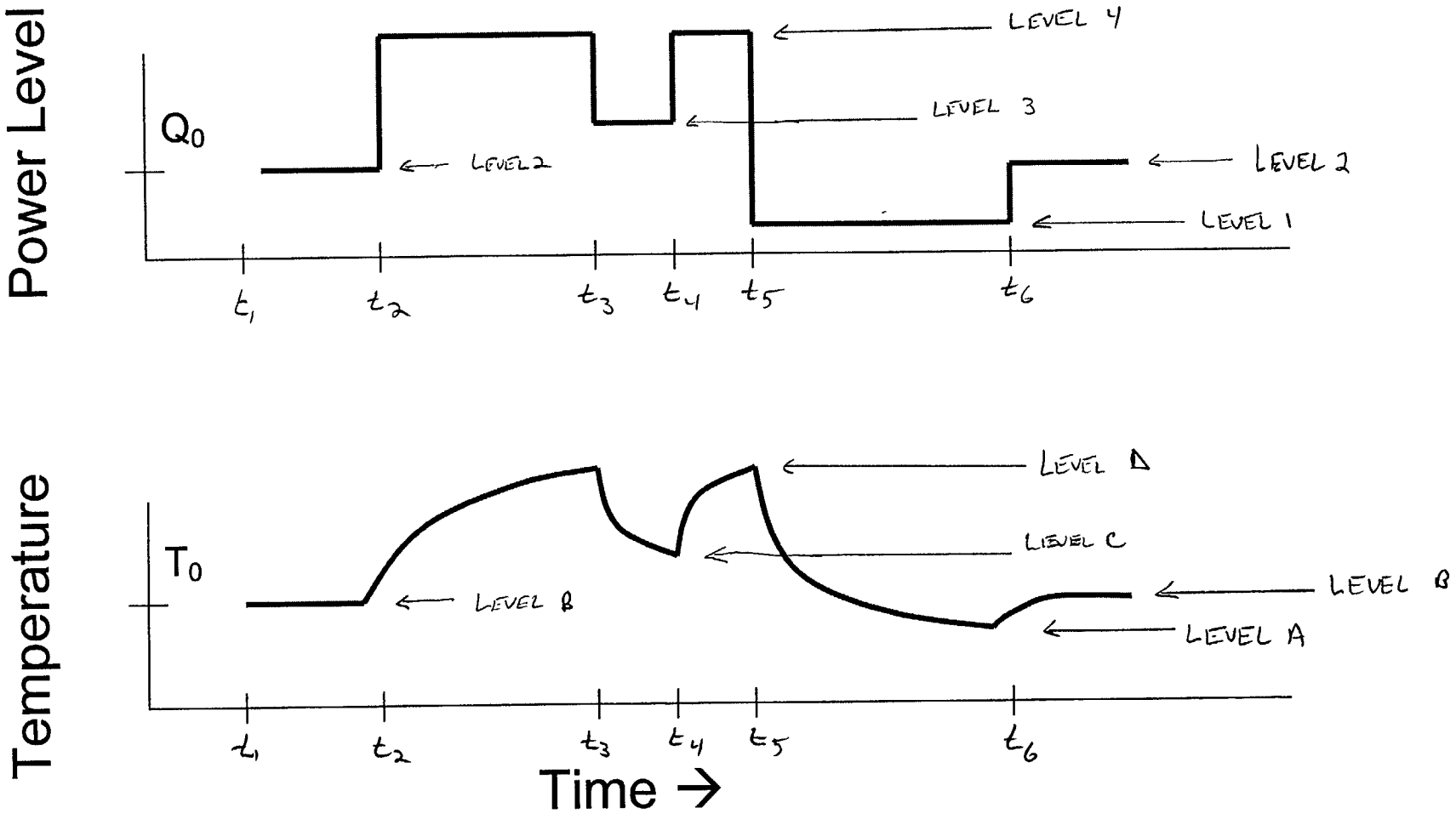

BEGIN
ACCESS SYSTEM ENVIRONMENT DATA
202
ACCESS MODULE DATA
204
DETERMINE SUSTAINABLE POWER LEVEL
206
TRANSLATE POWER LEVEL INTO MAX PERFORMANCE
208
ADJUST OPERATION OF IC SUCH THAT MAX PERFORMANCE CHAR. IS NOT EXCEEDED
210
END

FIG. 2

FIG. 3


Power Level
Q_0
LEVEL 4
LEVEL 3
LEVEL 2
LEVEL 2
LEVEL 1
t_1
t_2
t_3
t_4
t_5
t_6
Temperature
T_0
LEVEL D
LEVEL C
LEVEL B
LEVEL B
LEVEL A
t_1
t_2
t_3
t_4
t_5
t_6
Time →

Attorney's Docket No.: 42390.P7604 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DYNAMICALLY CONFIGURABLE THERMAL MANAGEMENT

the specification of which

X is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Aloysius T.C. AuYeung, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Aloysius T.C. AuYeung, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Lloyd L. Pollard II

Inventor's Signature _____ Date _____

Residence Portland, Oregon (City, State) Citizenship USA (Country)

Post Office Address 15295 NW Sweetgale Lane, Portland, Oregon 97229

Full Name of Second/Joint Inventor Nitin B. Gupte

Inventor's Signature _____ Date _____

Residence Beaverton, Oregon (City, State) Citizenship USA (Country)

Post Office Address 16795 NW Sandelie Court, Beaverton, Oregon 97006

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. P44,587; Thomas M. Coester, Reg. No. 39,637; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.